REMARKS

This amendment is being filed in response to the Office Action dated April 3, 2003. For the following reasons, this application should be considered in condition for allowance and the case passed to issue.

The drawings were objected to because of an informality. A substitute drawing figure has been submitted with the Amendment and a Request for Approval of Drawing Amendments filed on even date herewith. In this substitute figure, part 32 and part 34 on the left side of the gate electrode have been renumbered as pointed out by the Examiner to be consistent with the right side of the gate electrode. This conforms with the description in the specification and thus does not add new matter to the application. Approval of the drawing amendment change is respectfully requested.

Claims 1-2, 4, 6-10 were rejected under 35 USC §102 (b) as being anticipated by Ramaswami. Claims 3 and 11-17 were rejected under 35 USC §103(a) as being unpatentable over Ramaswami in view of Hong. Claim 5 was rejected under 35 USC §103(a) as being unpatentable over Ramaswami in view of Tseng et al. These rejections are hereby traversed and reconsideration and withdrawal thereof are respectfully requested. The following is a comparison of the present invention with the applied references.

The present invention, as recited claimed in amended claim 1, relates to a method of forming a semiconductor device and comprises the steps of forming a gate electrode on a substrate and a polysicilicon reoxidation layer over the substrate and the gate electrode. A nitride layer is deposited over the polysicilicon reoxidation layer, and the nitride layer is anisotropically etched. The etching stops on the polysilicon reoxidation layer to form nitride offset spacers on the gate electrode. Source/drain extensions are formed in the substrate

after the nitride layer has been etched. Sidewall spacers are subsequently formed in the offset spacers and source/drains are formed on the substrate.

The offset spacers help to reduce the overlap capacitance between the gate electrode and the drain, and thereby provide better AC performance for a transistor. The offset spacers separate the halo and the source/drain extension. The offset spacers are formed on the sides of the gate electrode. By forming a halo, followed by the formation of an offset spacers on the sidewalls of the gate electrode, and then formation of the source/drain extensions, the halo is physically located in front of the extensions. The use of the offset spacers makes the effective channel length longer for a given physical channel length. The problem of "gouging" in the conventional formation of offset spacers was described in the background of the present invention. The present invention avoids the gouging of the silicon substrate during the etching of the dielectric layer and formation of offset spacers by employing an etch stop layer, such as a polysilicon reoxidation layer. None of the references applied by the Examiner show or suggest the invention as now claimed.

Ramaswami, U.S. Patent No. 5,783,475, relates to a method of forming a spacer but fails to describe the invention identically as claimed. The present invention, as currently claimed, requires the source/drain extensions to be formed in the substrate after the nitride layer has been etched. This has importance in that the offset spacers, as described above, makes the effective channel length longer for a given physical channel length. Further, the use of the offset spacer in the present invention helps to separate the halo and the extension, in certain embodiments. This locates the halo physically in front of the source/drain extension. However, as clearly shown in the sequence of structures as depicted in figures 2-4 of Ramaswami, the source/drain extensions 34, 35 are formed prior to the depositing of

the nitride layer 36. For example, in figure 2, the source/drain extensions 34, 35 (the lightly doped source and drain regions) are created by lightly doped source and drain implantation through the dielectric layer 48 into the semiconductor or substrate 31. See column 2, lines 56-63 of Ramaswami. It is only after the formation of the lightly doped source/drain regions 34, 35, that the nitride layer 36 is deposited in figure 3. Etching is performed in figures 4 and 5 to remove portions of the nitride layer 36. This etching, however, is performed only after source/drain extensions are already formed. Hence, the nitride layer 36 is not employed as an offset spacer in the same meaning as in the present invention. There is no offset of the source/drain extensions created by the nitride spacers, since the implantation of the source/drain regions 34, 35 is performed prior to the etching of the nitride layer 36.

Since Ramaswami fails to identically disclose each and every step or element of the claimed invention, it cannot anticipate the claims under 35 USC §102(b). Accordingly, reconsideration and withdrawal of the rejection of claims 1-2, 4 and 6-10 under 35 USC §102(b) are respectfully requested. The remaining rejections of the dependent claims under 35 USC §103(a) based upon combinations of Ramaswami with Hong and with Tseng et al., should also be reconsidered and withdrawn since neither Hong nor Tseng et al. overcome any of the deficiencies noted with respect to claims 1 and 11, and the dependent claims further limit and define the amended independent claims. Reconsideration and withdrawal of the rejections of claims 3, 5 and 11-17 under 35 USC §103(a) are therefore respectfully requested.

In light of the amendments and remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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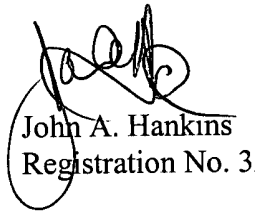

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Date: May 12, 2003